

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.	Application No.			
				MST-1898-22D	10/800,382			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicants				
				Leung et al.				
AUG 02 2004 PATENT & TRADEMARK OFFICE				Filing Date	Group			
				3/11/2004	Unknown			
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
JT	AA	3,585,378	15 May 1971	Bouricius et al.				
↑	AB	3,651,473	21 Mar 1972	Faber				
	AC	3,761,879	25 Sep 1973	Brandsma et al.				
	AD	3,803,562	9 Apr 1974	Hunter				
	AE	3,810,301	14 May 1974	Cook				
	AF	3,835,530	17 Sep 1974	Kilby				
	AG	3,849,872	26 Nov 1974	Hubacher				
	AH	3,859,640	7 Jan 1975	Eberlein et al.				
	AI	3,983,537	28 Sep 1976	Parsons et al.				
↓	AJ	4,007,452	8 Feb 1977	Hoff, Jr.				
JT	AK	4,038,648	26 Jul 1977	Chesley				
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JT		Document	Date	Country	Class	Subclass	Yes	No
↑	AL	1002664	28 Dec 1976	Canada				
	AM	0162932 A3	4 Dec 1985	EP				
	AN	0178949 A3	23 Apr 1996	EP				
↓	AO	0258062 A2	2 Mar 1988	EP				
JT	AP	0258062 A3	2 Mar 1988	EP				
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JT	AQ	"32K x9 Bit BurstRAM Synchronous Static RAM with burst Counter and Self-Timed Write," Motorola Memory Data (MCM62486A)(No Date), pp. 7-100 to 7-109.						
JT	AR	Antola et al., "Reconfiguration of Binary Trees: The Flow-Driven Approach," 1991 International Conference on Wafer Scale Integration, 1991, pp. 141-147.						
JT	AS	Aubusson, Russell C. and Ivor Catt, "Wafer-Scale Integration-A Fault-Tolerant Procedure," IEEE Journal of Solid State Circuits, Vol. SC-13, No. 3, Jun 1978, pp. 339-344.						
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	AB	4,071,887	2 Jan 1978	Daly et al.			
	AC	4,092,733	30 May 1978	Coontz et al.			
	AD	4,132,869	2 Jan 1979	Knox			
	AE	4,188,670	12 Feb 1980	Hsia			
	AF	4,215,430	29 Jul 1980	Johnson, Jr.			
	AG	4,227,045	7 Oct 1980	Chelcun et al.			
	AH	4,236,087	25 Nov 1980	Kaminski et al.			
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	AJ	4,329,685	11 May 1982	Mahon et al.			
JT	AK	4,355,387	19 Oct 1982	Portejoie et al.			

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JT	AL	0313040 A2	26 Apr 1989	EP				
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	AN	0389203 A2	29 Sep 1990	EP				
	AO	0440456 A3	7 Aug 1991	EP				
JT	AP	0504434 A1	23 Sep 1992	EP				

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JT	AQ	Cavil et al., "Wafer-Scale Integration," Microelectronics Manufacturing Technology, May 1991, pp. 55-59.
JT	AR	Fujii, et al., "A 50- $\mu$ A Standby 1M x1/256K x4 CMOS DRAM with High-Speed Sense Amplifier," IEEE Journal of Solid State Circuits, Vol. SC-21, No. 5, Oct 1986, pp. 643-647.
JT	AS	Ganapathy et al., "Yield Optimization in Large RAM's with Hierarchical Redundancy," IEEE Journal of Solid-State Circuits, Vol. 26, No. 9, Sep 1991, pp. 1259-1269.

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	AB	4,400,794	23 Aug 1983	Koos			
	AC	4,407,014	27 Sep 1983	Holtey et al.			
	AD	4,414,480	8 Nov 1983	Zasio			
	AE	4,438,352	20 Mar 1984	Mardkha			
	AF	4,458,297	3 Jul 1984	Stopper et al.			
	AG	4,467,400	21 Aug 1984	Stopper			
	AH	4,494,196	15 Jan 1985	Greer			
	AI	4,605,928	12 Aug 1986	Georgiou			
▼	AJ	4,612,613	16 Sep 1986	Gershenson et al.			
JT	AK	4,615,017	30 Sep 1986	Finlay et al.			

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	AM	0540363 A1	5 May 1993	EP				
	AN	0606600 A1	20 Jul 1994	EP				
▼	AO	52-30095	8 May 1977	Japan			X (Cum)	
JT	AP	56-501547	22 Oct 1981	Japan			X (Abst)	

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JT	AQ	Herbert Stopper, "Wafer-Scale Integration," in <i>Hybrids and High-Level Integration</i> , (No Date) pp. 354-364.
JT	AR	Horst, Robert W., "Task-Flow Architecture for WSI Parallel Processing," <i>IEEE Trans Jnl</i> , Apr. 1992, pp. 10-18.
JT	AS	IBM Technical Disclosure Bulletin, "Mixed Voltage Protection" Vol. 32, No. 5A, Oct. 1989, pp. 423-425.

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JT	AA	4,627,058	2 Dec 1986	Moriyama			
	AB	4,630,355	23 Dec 1986	Johnson			
	AC	4,637,073	13 Jan 1987	Selin et al.			
	AD	4,639,861	27 Jan 1987	Appiano et al.			
	AE	4,639,933	27 Jan 1987	Howell et al.			
	AF	4,644,502	17 Feb 1987	Kawashima			
	AG	4,646,298	24 Feb 1987	Laws et al.			
	AH	4,649,384	10 Mar 1987	Sheafor et al.			
	AI	4,653,050	24 Mar 1987	Vaillancourt			
	AJ	4,663,758	5 May 1987	Lambarelli et al.			
▼	AK	4,667,328	19 May 1987	Imran			
JT	AL	4,680,780	14 Jul 1987	Agoston et al.			

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		Document	Date	Country	Class	Subclass	Yes	No
JT	AM	59-4798	31 Jan 1984	Japan				X
	AN	59-212962	1 Dec 1984	Japan			X (Abst)	
	AO	60-73774	25 Apr 1985	Japan			X (Abst)	
▼	AP	60-95641	29 May 1985	Japan			X (Abst)	
JT	AQ	60-98790	1 Jun 1985	Japan			X (Abst)	

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JT	AR	IBM Technical Disclosure Bulletin, "Bi-CMOS-Volt Tri-State Drive With 5-Volt Interface Capability", Vol. 32, No. 9A, Feb. 1990, pp. 405-406.
JT	AS	MacDonald et al, "Fabrication: 200Mb Wafer Memory," IEEE International Solid-State Circuits Conference (Feb 1989), pp. 240-241 and 350.
JT	AT	Peter van Zant, Microchip Fabrication: A Practical Guide to Semiconductor Processing, (1 <sup>st</sup> ed., 1986), p. 8.

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	AB	4,707,808	17 Nov 1987	Heimbigner			
	AC	4,719,621	12 Jan 1988	May			
	AD	4,736,365	5 Apr 1988	Stern			
	AE	4,748,588	31 May 1988	Norman et al.			
	AF	4,769,789	6 Sep 1988	Noguchi et al.			
	AG	4,782,457	1 Nov 1988	Cline			
	AH	4,785,415	15 Nov 1988	Karlquist			
	AI	4,823,363	18 Apr 1989	Yoshida			
V	AJ	4,839,909	13 Jun 1989	Warner			
JT	AK	4,847,615	11 Jul 1989	McDonald			

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JT	AL	60-186940	24 Sep 1985	Japan			X (Abst)	
	AM	63-246843	13 Oct 1988	Japan			X (Abst)	
	AN	63-268020	4 Nov 1988	Japan			X (Abst)	
	AO	64-19745	23 Jan 1989	Japan			X (Abst)	
V	AP	64-25626	27 Jan 1989	Japan			X (Abst)	
JT	AQ	1-138687	31 May 1989	Japan			X (Abst)	

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JT	AR	Rhodes et al., "A Monolithic Hough Transform Processor Based on Restructurable VLSI," IEEE Trans. on Pattern Analysis and Machine Intelligence, Vol. 10, No. 1 (Jan 1988), pp. 106-110.
JT	AS	Ron Iscoff, "Characterizing Quickturn ASICs: It's Done with Mirrors" Semiconductor International, Aug. 1, 1990, pp. 68-73.
JT	AT	Shi, Weiping and W. Kent Fuchs, "Large Area Defect-Tolerant Tree Architectures," 1991 International Conference on Wafer Scale Integration, 1991, pp. 127-133.

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	AB	4,860,285	22 Aug 1989	Miller et al.			
	AC	4,864,496	5 Sep 1989	Triolo et al.			
	AD	4,866,508	12 Sep 1989	Eichelberger et al.			
	AE	4,872,137	3 Oct 1989	Jennings, III			
	AF	4,876,700	24 Oct 1989	Grindahl			
	AG	4,881,232	14 Nov 1989	Sako et al.			
	AH	4,884,122	28 Nov 1989	Eichelberger et al.			
	AI	4,890,224	26 Dec 1989	Fremont			
↓	AJ	4,897,818	30 Jan 1990	Redwine et al.			
JT	AK	4,906,987	6 Mar 1990	Venaleck et al.			

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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
JT	AL	U.M. 2-116346	18 Sep 1990	Japan				X
	AM	2 246099 A	1 Oct 1990	Japan			X (Abst)	
	AN	2-246445	2 Oct 1990	Japan			X (Abst)	
↓	AO	3-502845	27 Jun 1991	Japan			X (Abst)	
JT	AP	3-201551	3 Sep 1991	Japan			X (Cum)	

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JT	AQ	Stodieck, Robert, "Designing With the IDT49C460 and IDT39C60 Error Detection and Correction Units," Application Note AN-24 by Integrated Device Technology, Inc., 1993, pp. 1-10.
JT	AR	Takai et al., "250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture," IEEE Journal of Solid State Circuits, Vol. 29, No. 4, Apr. 1994, pp. 426-431.
JT	AS	Yamashita, Koichi and Shohei Ikebara, "A Design and Yield Evaluation Technique for Wafer-Scale Memory," IEEE Trans Jnl, Apr. 1992, pp. 19-27.

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	AB	4,912,633	27 Mar 1990	Schweizer et al.			
	AC	4,926,382	15 May 1990	Sakui et al.			
	AD	4,937,203	26 Jun 1990	Eichelberger et al.			
	AE	4,943,914	24 Jul 1990	Kubo			
	AF	4,943,966	24 Jul 1990	Giunta et al.			
	AG	4,954,854	4 Sep 1990	Dhong et al.			
	AH	4,955,020	4 Sep 1990	Stone et al.			
	AI	4,961,169	2 Oct 1990	Matsumura et al.			
	AJ	4,970,724	13 Nov 1990	Yung			
↓	AK	4,974,048	27 Nov 1990	Chakravorty et al.			
JT	AL	4,980,765	25 Dec 1990	Kudo et al.			

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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
JT	AM	3-204957	6 Sep 1991	Japan			X (Abst)	
	AN	WO 81/01893	9 Jul 1981	WIPO				
	AO	WO 90/04576	3 May 1990	WIPO				
↓	AP	WO 90/07153	28 Jun 1990	WIPO				
JT	AQ	WO 90/09635	23 Aug 1990	WIPO				

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	AS	
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		3/11/2004	Unknown

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	AB	4,985,895	15 Jan 1991	Pelkey			
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	AE	5,008,882	16 Apr 1991	Peterson et al.			
	AF	5,020,020	28 May 1991	Pomfret et al.			
	AG	5,021,985	14 Jun 1991	Hu et al.			
	AH	5,043,820	27 Aug 1991	Wyles et al.			
	AI	5,045,725	3 Sep 1991	Sasaki et al.			
	AJ	5,051,938	24 Sep 1991	Hyduke			
	AK	5,055,897	8 Oct 1991	Canepa et al.			
↓	AL	5,077,596	31 Dec 1991	Inoue			
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JT	AN	WO 91/16680	31 Oct 1991	WIPO				
	AO	WO 92/08193	14 May 1992	WIPO				
	AP	WO 93/18459	16 Sep 1993	WIPO				
↓	AQ	WO 93/18462	16 Sep 1993	WIPO				
JT	AR	WO 93/18463	16 Sep 1993	WIPO				

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	AG	5,226,147	6 Jul 1993	Fujishima et al.				
	AH	5,227,677	13 Jul 1993	Furman				
	AI	5,243,623	7 Sep 1993	Murdock				
↓	AJ	5,243,703	7 Sep 1993	Farmwald et al.				
JT	AK	5,247,522	21 Sep 1993	Reiff				
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	AM						No	
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	AS							
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	AB	5,252,507	12 Oct 1993	Hively et al.				
	AC	5,254,883	19 Oct 1993	Horowitz et al.				
	AD	5,261,077	9 Nov 1993	Duval et al.				
	AE	5,265,216	23 Nov 1993	Murphy et al.				
	AF	5,267,200	30 Nov 1993	Tobita				
	AG	5,268,639	7 Dec 1993	Gasbarro et al.				
	AH	5,278,967	11 Jan 1994	Curran				
	AI	5,297,092	22 Mar 1994	Johnson				
	AJ	5,301,152	5 Apr 1994	Iwashita				
V	AK	5,311,083	10 May 1994	Wanlass				
JT	AL	5,317,540	31 May 1994	Furuyama				
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	AN							
	AO							
	AP							
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	AR							
	AS							
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	AB	5,329,174	12 Jul 1994	Chiang			
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	AF	5,379,258	3 Jan 1995	Murakami et al.			
	AG	5,402,388	28 Mar 1995	Wojcicki et al.			
	AH	5,420,824	30 May 1995	Kajimoto et al.			
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▼	AJ	5,465,223	7 Nov 1995	Nishimura			
JT	AK	5,498,886	12 Mar 1996	Hsu et al.			

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
JT	AA	5,561,630	1 Oct 1996	Katoh et al.				
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		Document	Date	Country	Class	Subclass	Yes	No
	AL							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ							
	AR							
	AS							
Examiner /Joseph Torres/			Date Considered 10/25/2006					
<p><b>*EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								